EXPERIMENT 1

Digital to Analog (DAC) Conversion

OBJECTIVE

Purpose of the experiment is to obtain analog voltage and/or current from digital signal.

EQUIPMENT REQUIRED

Components

1*LF351 OPAMP
5*20KΩ
15*10KΩ
4*switch

PRELİMİNARY WORK

Study OPAMP summing amplifiers and review how to use it as a Digital to Analog Converter (DAC) by binary weighted resistors and R-2R ladder arrangement.

BACKGROUND INFORMATION

A digital to analog converter (DAC) converts a digital signal to an analog voltage or current output. Many types of DACs are available and usually switches, resistors, and op-amps are used to implement the conversion. In Figure 1, a summing amplifer with binary weighted resistors are given.

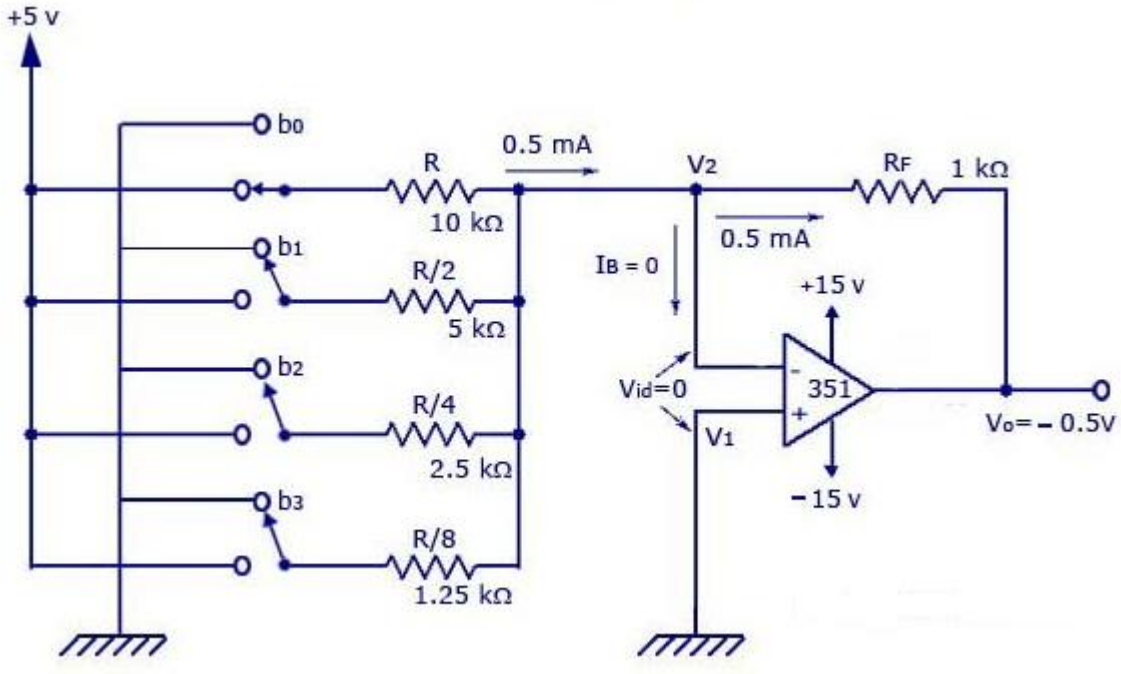

Figure 1. DAC by opamp summing amplifer with binary weighted resistors

R-2R Ladder is another type of DAC based on the opamp summing amplifier similarly as seen in Figure 2. Each bit corresponds to a switch:

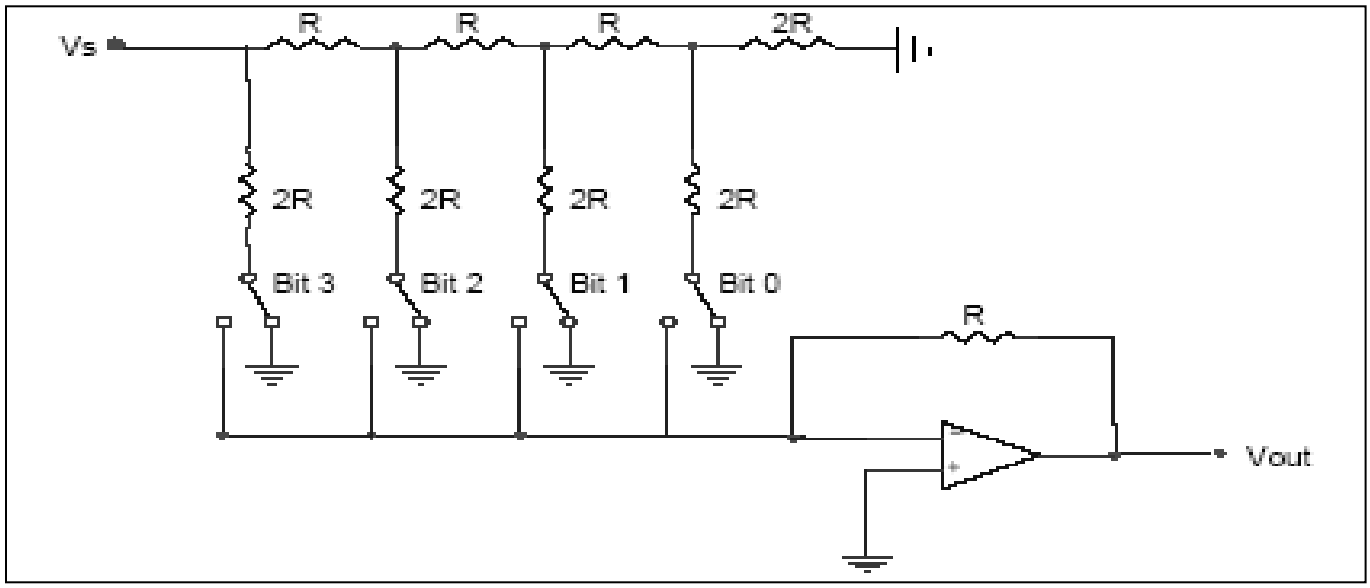

Figure 2. DAC by R-2R Ladder

If the bit is high, the corresponding switch is connected to the inverting input of the op-amp. If the bit is low, the corresponding switch is connected to ground.

*b*n means Bit n, hence;

If bit n is set, *b*n=1
If bit n is clear, *b*n=0

For a 4-Bit R-2R Ladder, output is equal to;

$$V_{\text{out}} = -V_{\text{ref}}\left(b_3\frac{1}{2} + b_2\frac{1}{4} + b_1\frac{1}{8} + b_0\frac{1}{16}\right)$$

For general n-Bit R-2R Ladder , output is equal to;

$$V_{\text{out}} = -V_{\text{ref}}\sum_{i=1}^{n} b_{n-i}\frac{1}{2^i}$$

Experimental Procedure:

1) Construct the circuit in Figure 1 and fill in Table 1 (use 10k resistors in parallel configurations).
2) Construct the circuit in Figure 3 and fill in Table 2.

Table 1. Results for the circuit in Figure 1.

Sw0	*Sw1*	*Sw2*	*Sw3*	i_{out}	v_o
closed	*open*	*open*	*open*		
open	*closed*	*open*	*open*		
closed	*closed*	*open*	*open*		
open	*open*	*closed*	*open*		
closed	*open*	*closed*	*open*		
open	*closed*	*closed*	*open*		
closed	*closed*	*closed*	*open*		
open	*open*	*open*	*open*		
closed	*open*	*open*	*closed*		
open	*closed*	*open*	*closed*		
closed	*closed*	*open*	*closed*		
open	*open*	*closed*	*closed*		
closed	*open*	*closed*	*closed*		
open	*closed*	*closed*	*closed*		
closed	*closed*	*closed*	*closed*		

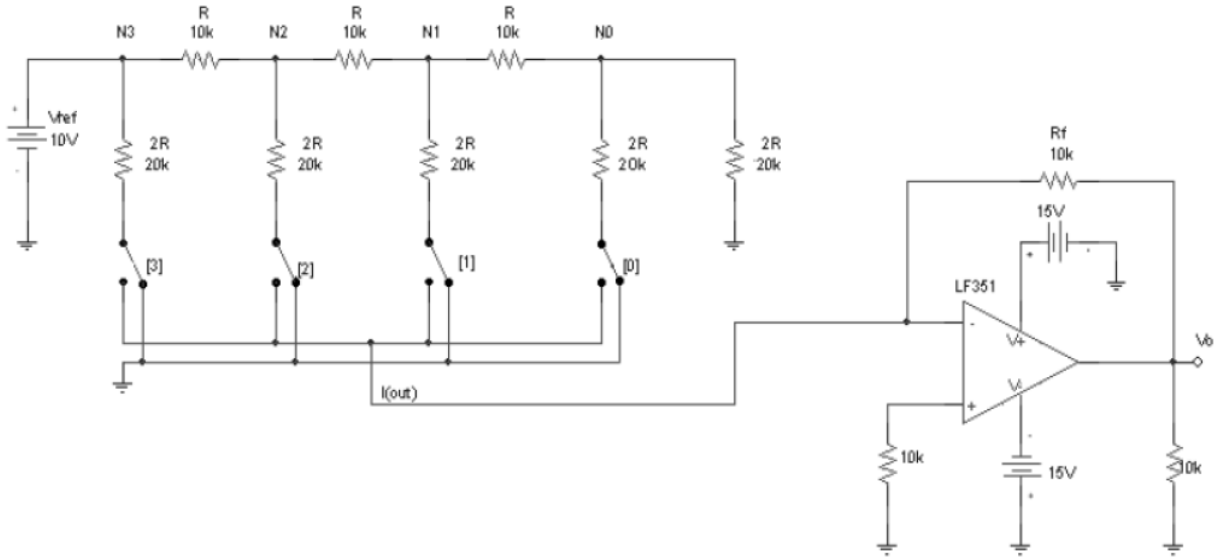

Figure 3. R-2R ladder circuit to be constructed

Table 2. Results for the circuit in Figure 3.

Sw0	*Sw1*	*Sw2*	*Sw3*	i_{out}	v_o
closed	*open*	*open*	*open*		
open	*closed*	*open*	*open*		
closed	*closed*	*open*	*open*		
open	*open*	*closed*	*open*		
closed	*open*	*closed*	*open*		
open	*closed*	*closed*	*open*		
closed	*closed*	*closed*	*open*		
open	*open*	*open*	*open*		
closed	*open*	*open*	*closed*		
open	*closed*	*open*	*closed*		
closed	*closed*	*open*	*closed*		
open	*open*	*closed*	*closed*		
closed	*open*	*closed*	*closed*		
open	*closed*	*closed*	*closed*		
closed	*closed*	*closed*	*closed*		

Conclusion : Compare ideal and experimental results. What is the rate of the difference? Explain its reasons.